UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,621	04/22/2004	David Arnold Luick	ROC920030202US1	7313

7590 05/11/2006

Robert R. Williams
IBM Corporation, Dep. 917
3605 Highway 52 North
Rochester, MN 55901-7829

EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 05/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,621	LUICK, DAVID ARNOLD	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 9-10, 12 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Hironaka et al (US PGPub No. 20040088489).

For claim 1, Hironaka discloses a digital data processing device, comprising:

instruction logic which selects and decodes instructions for execution (a selection circuit which selects one set of data which is required by the processor among sets of data read from a plurality of selected banks through the output port for usual data, par. 0203);

execution logic which executes instructions (each instruction issued from the integrated cache is executed by an execution unit, par. 0132);

a first cache for temporarily storing data, said first cache comprising a plurality of banks, each bank containing at least one respective access port for accessing data in the bank (a multi-port instruction and trace integrated cache with a plurality of banks, par. 0131); and

wherein a respective bank predict value is associated with each of at least some instructions accessing said first cache, each said bank predict value predicting a bank of said first cache to be accessed by its associated instruction (a predict path inputted from a branch predictor, par. 0131; when the integrated cache adopts a bank structure, since the trace data is stored in each bank, a trace is generated by fetching banks according to a branch predict from a plurality of the banks, par. 0146); and

wherein said instruction logic selects multiple instructions for concurrent execution, said instruction logic using said bank predict values of said instructions to select multiple instructions which access said first cache for concurrent execution (the multi-port instruction and trace integrated cache simultaneously fetches and issues instructions from a plurality of banks provided inside the cache, par. 0131; par. 0146).

For claim 3, Hironaka discloses each said bank of said first cache contains a plurality of read ports and at least one write port (a plurality of banks and a plurality of ports including an instruction port unit consisting of at least one port used to have access to an instruction from the parallel processor, and a data port unit consisting of at least one data port used to have access to data from the parallel processor, par. 0028).

Claim 9 is rejected using the same rationale as for the rejection of claim 1 above.

For claim 10, Hironaka discloses the invention as per rejection of claim 1 above.

Hironaka further discloses a memory (a main memory which stores programs or various kinds of data or information, par. 0003); and

at least one processor, said processor communicating with said memory over at least one communications path, said processor including instruction logic for selecting

and decoding instructions for execution, and execution logic for executing instructions (a parallel processor to execute a plurality of types of processing and a main memory, par. 0028).

Claim 12 is rejected using the same rationale as for the rejections of claims 3 and 10 above.

Claim 20 is rejected using the same rationale as for the rejection of claim 10 above.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hironaka et al (US PGPub No. 20040088489) and Nakamura (US PGPub No. 20020152368).

For claim 2, Hironaka discloses the invention as per rejection of claim 1 above.

Hironaka fails to disclose the limitations of the current claim.

Nakamura, however, helps disclose a second cache for temporarily storing data, wherein said second cache stores instructions executable by said execution logic and said first cache stores data other than instructions, and wherein said bank predict values are stored in said second cache (instructions are arranged to include a field to

contain a value that indicates whether to perform value prediction, par. 0011; in an instruction cache, for the instruction for which a value was predicted, the data contents of its value prediction field or value prediction method field are updated accordingly, par. 0047).

Hironaka and Nakamura are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a second cache for storing instructions and bank predict values because this would make it possible to specify an instruction for which value prediction is thought to enhance program execution performance, and would enhance the accuracy of prediction when carrying out value prediction (par. 0000-0010), as taught by Nakamura.

Claim 11 is rejected using the same rationale as for the rejections of claims 2 and 10 above.

5. Claims 4-5, 7-8, 13-14 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hironaka et al (US PGPub No. 20040088489) and Biles (US PGPub No. 20040210749).

For claim 4, Hironaka discloses the invention as per rejection of claim 1 above.

Hironaka fails to disclose the limitations of the current claim.

Biles, however, helps disclose a respective confirmation value is associated with each said instruction with which a bank predict value is associated, each confirmation value reflecting a degree of confidence in the respective bank predict value (a

confirmation signal indicates that an instruction is a branch instruction, and control logic will be arranged to output the prediction information to identify to the address generation logic whether or not the branch is to be predicted as taken, par. 0085).

Hironaka and Biles are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a instruction confirmation values for bank predict values and applying these to multiple instructions for concurrent execution because this would allow for simultaneous access to a plurality of sets of information from memory (par. 0007) as taught by Hironaka, and provide a method of generating within a data processing apparatus a branch bias providing a prediction as to whether execution of a branch instruction will result in a branch being taken or not taken (par. 0047), as taught by Biles.

For claim 5, the combined teachings of Hironaka and Biles disclose the invention as per rejection of claim 4 above.

Biles further helps disclose said digital data processing device dynamically maintains said confirmation values (history information is input to index generation logic, which is also arranged to receive the address of an instruction whose branch behavior is to be predicted, par. 0007).

For claim 7, the combined teachings of Hironaka and Biles disclose the invention as per rejection of claim 5 above.

Biles further helps disclose feedback logic which maintains bank prediction history data in a form accessible to a programmer, said bank prediction history data

recording the performance of bank predictions by said bank predict values during execution of a computer program (a history storage operable to store history data identifying an outcome for a number of preceding branch instructions, par. 0016).

For claim 8, the combined teachings of Hironaka and Biles disclose the invention as per rejection of claim 5 above.

Biles further helps disclose said instruction logic concurrently selects and decodes instructions for execution from a plurality of threads (branch identification logic further includes decode logic which is arranged to perform some preliminary decode of instructions in the instruction buffer, par. 0086).

Claim 13 is rejected using the same rationale as for the rejections of claims 4 and 10 above.

Claim 14 is rejected using the same rationale as for the rejections of claims 5 and 10 above.

Claim 16 is rejected using the same rationale as for the rejections of claims 7 and 10 above.

Claim 17 is rejected using the same rationale as for the rejections of claims 8 and 10 above.

6. Claims 6 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hironaka et al (US PGPub No. 20040088489), Biles (US PGPub No. 20040210749) and Rappoport et al (US PGPub No. 20050262332).

For claim 6, the combined teachings of Hironaka and Biles disclose the invention as per rejection of claim 4 above.

These teachings fail to disclose the limitations of the current claim.

Rappoport, however, helps disclose each said confirmation value is a counter which is incremented for each correct bank prediction and decremented for each incorrect bank prediction (each misprediction results in a counter being decremented, and each correct prediction results in the counter being incremented, par. 0105).

Hironaka, Biles and Rappoport are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a counter for bank predictions because this would provide an indication of the number of times a prediction has been correct or incorrect for a particular branch (par. 0105), as taught by Rappoport.

Claim 15 is rejected using the same rationale as for the rejections of claims 6 and 10 above.

7. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hironaka et al (US PGPub No. 20040088489) and Arimilli et al (US Patent No. 6,629,268).

For claim 18, Hironaka discloses the invention as per rejection of claim 10 above.

Hironaka fails to disclose the limitations of the current claim.

Arimilli, however, helps disclose said computer system comprises a plurality of caches at different cache levels, said first cache being at a level closest said processor (multiprocessor system with multi-level cache memories where typically each higher level is smaller and has a shorter access time; both data and instructions may be cached, and data and instruction cache entries are typically loaded by prefetch units and branch prediction units before they are needed by an execution unit, col. 1, lines 27-35).

For claim 19, the combined teachings of Hironaka and Arimilli disclose the invention as per rejection of claim 18 above.

Arimilli further helps disclose said computer system comprises a plurality of said processors, each processor being coupled to a respective first cache, and wherein said bank predict values associated with instructions are maintained in a location accessible to each of said plurality of processors (col. 1, lines 27-35).

Citation of Pertinent Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shen et al (US PGPub No. 20050182907) discloses a novel cache residence prediction mechanism that predicts whether requested data of a cache miss can be found in another cache.

Contact Information

9. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

5-9-06

Pierre Vital

PIERRE VITAL
PRIMARY EXAMINER